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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/902,756	07/12/2001	Nobuyuki Hirayama	862.C2290	9593

5514 7590 03/14/2005

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EXAMINER	
THOMPSON, JAMES A	
ART UNIT	**PAPER NUMBER**
2624	

DATE MAILED: 03/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/902,756	HIRAYAMA, NOBUYUKI	
	Examiner	Art Unit	
	James A Thompson	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☒ Claim(s) *1-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification/Drawings

1. Examiner has thoroughly reviewed the specification and drawings and has not found any errors. However, given the length of the specification and the number and detail of the drawings, Applicant is advised to thoroughly review the specification and drawings to ensure their accuracy.

Claim Objections

2. Claims 1-6 are objected to because of the following informalities:

In claim 1, line 7, "and said printhead including," should be changed to "said printhead including:" in order to be in the proper format.

In claim 1, line 10, "each group," should be changed to "each group;" in order to be in the proper format.

Claim 1, lines 11-14 does not use appropriate claim language. Specifically, in lines 13-14, "plurality of paths are arranges on the substrate" should be modified to "plurality of paths, which are arranged on the substrate" or "plurality of paths, wherein said data supply circuits are arranged on the substrate" or "plurality of paths, wherein said data supply circuits and said plurality of paths are arranged on the substrate". The grammar of the limitation corresponding to the data supply circuits as currently written does not correspond with proper claim format since the grammar of said limitation seems to describe what the data supply circuit is rather than what it does. Further, the grammar of the claim does not make

clear whether the data supply circuit, the plurality of paths, or both are arranged on the substrate.

In claim 6, line 3, "thermal energy, and comprises an" should be changed to "thermal energy; and an" since "comprises" is already implied by the use of "includes" in line 2.

Claims 2-5 depend from claim 1 and are therefore also objected to.

Appropriate correction is required.

3. Claim 7 is objected to because of the following informalities:

In claim 7, line 7, "and said printhead includes," should be changed to "and wherein said printhead includes:" in order to be in proper claim format.

Appropriate correction is required.

4. Claim 8 is objected to because of the following informalities:

In claim 8, lines 6-7, "and the printhead including" should be changed to "and wherein the printhead includes:" in order to be in proper claim format.

In claim 8, line 13, "substrate, comprising" should be changed to "substrate, comprising:" in order to be in proper claim format.

Appropriate correction is required.

5. Claim 9 is objected to because of the following informalities:

In claim 9, lines 7-8, "and the printhead element substrate including," should be changed to "and wherein the printhead

element substrate includes:" in order to be in proper claim format.

Claim 9, lines 12-15 does not use appropriate claim language. Specifically, in lines 14-15, "plurality of paths are arranges on the substrate" should be modified to "plurality of paths, which are arranged on the substrate" or "plurality of paths, wherein said data supply circuits are arranged on the substrate" or "plurality of paths, wherein said data supply circuits and said plurality of paths are arranged on the substrate". The grammar of the limitation corresponding to the data supply circuits as currently written does not correspond with proper claim format since the grammar of said limitation seems to describe what the data supply circuit is rather than what it does. Further, the grammar of the claim does not make clear whether the data supply circuit, the plurality of paths, or both are arranged on the substrate.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 8 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art

to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 8 recites a printing apparatus comprising driving data generation means. The rest of the claim can be considered the preamble, and thus claim 8 does not recite any other means. Therefore, claim 8 is a single means claim. A single means claim, i.e., where a means recitation does not appear in combination with another recited element of means, is subject to an undue breadth rejection under 35 U.S.C. §112, first paragraph (*In re Hyatt*, 708 F.2d 712, 714-715, 218 USPQ 195, 197 (Fed. Cir. 1983)). A single means claim which covered every conceivable means for achieving the stated purpose was held nonenabling for the scope of the claim because the specification disclosed at most only those means known to the inventor. When claims depend on a recited property, a fact situation comparable to Hyatt is possible, where the claim covers every conceivable structure (means) for achieving the stated property (result) while the specification discloses at most only those known to the inventor. Applicant is referred to MPEP §2164.08(a).

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1-6 and 9 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 and 9 both recite "a selection circuit ... and data supply circuits for supplying driving data to the driving

circuit for driving each printing element through any of a plurality of paths are arranged on the substrate." This claim language is confusing. Does Applicant mean that the data supply circuits are arranged on the substrate, or the plurality of paths are arranged on the substrate, or the selection circuit and the data supply circuits are arranged on the substrate, or some combination therein? The language of claims 1 and 9, as currently written, is confusing and indefinite with regards to this question. Claims 2-6 depend from claim 1 and are therefore also rejected under 35 U.S.C. §112, second paragraph.

10. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 7 recites the limitation "the printhead" in line 2. There is insufficient antecedent basis for this limitation in the claim.

11. Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 recites the limitation "the printhead" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Further, the language of claim 8 does not make it clear if the printhead, along with the selection circuits and data supply circuits comprising the printhead, are included as part of the overall printing apparatus. The language of claim 8 could be

interpreted to mean that the printing apparatus merely uses the printhead, but said printhead is not a part of the overall printing apparatus.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 1-2 and 4-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai (US Patent 5,539,433) in view of Tamura (European Patent Application Publication EP 0 811 488 A2).

Regarding claim 1: Kawai discloses a printhead (figure 1 of Kawai) in which a plurality of printing elements (figure 1 (10) and column 3, lines 34-36 of Kawai) arranged in a predetermined direction (column 3, lines 29-33 of Kawai) and a driving circuit (figure 1(50) of Kawai) for driving the printing elements (column 4, lines 35-41 of Kawai) are formed on a single substrate (figure 1 and figure 2 of Kawai). The thermal head (figure 1(10) of Kawai) contains a plurality of printing elements since said thermal head prints a plurality of primary colors (column 3, lines 29-36 of Kawai). Said printing elements are set according to specific positions (column 3, lines 29-33 of Kawai), and therefore must be set in a predetermined direction. The plurality of printing elements (figure 1 (10) of

Kawai) are shown in figure 2 of Kawai (column 2, lines 15-16 of Kawai), and are clearly a single substrate.

Kawai further discloses that said printhead includes data supply circuits (figure 1(5) of Kawai) for supplying driving data to the driving circuit (column 4, lines 45-48 of Kawai) for driving each printing element through any of a plurality of paths (column 4, lines 47-55 of Kawai). Said data supply circuits are a part of the overall directly connected digital logic circuitry (figure 1 and column 3, lines 21-25 of Kawai). Therefore, said data supply circuits are arranged on the substrate.

Kawai does not disclose expressly that the printing elements are classified into a plurality of groups; and a selection circuit which is common to the plurality of groups and selects a printing element to be driven in each group, wherein said selection circuit is arranged on the substrate.

Tamura discloses classifying printing elements into a plurality of groups (column 5, lines 44-51 of Tamura); and a selection circuit (figure 2 of Tamura) which is common to the plurality of groups (column 5, lines 19-20 of Tamura) and selects a printing element to be driven in each group (column 5, lines 49-51 and column 6, lines 16-20 of Tamura).

Kawai and Tamura are combinable because they are from the same field of endeavor, namely the digital control of printheads and printhead data. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the plurality of groups and a selection circuit to select a printing element from each group, as taught by Tamura, in the overall printhead taught by Kawai. Since the printhead of Kawai is a single integrated device (figure 1 of Kawai), the selection

circuit taught by Tamura would also be arranged on the substrate, said substrate being the substrate that is inherently required to form a physical digital circuit. The motivation for doing so would have been that constant switching of power components creates a large power loss and requires bulky circuits (column 2, lines 44-57 of Tamura) and using a diode or transistor matrix requires a disadvantageous number of wiring lines, which increases cost and degrades reliability (column 2, line 58 to column 3, line 7 of Tamura). Both of these problems are solved by using the selection circuit taught by Tamura (column 3, lines 11-14 of Tamura). Therefore, it would have been obvious to combine Tamura with Kawai to obtain the invention as specified in claim 1.

Regarding claim 2: Kawai discloses that the data supply circuits (figure 1(5) of Kawai) supply the driving data through a direct path (figure 1(5,50); figure 2; and column 3, lines 21-25 of Kawai). As can be clearly seen in figure 1 of Kawai, the data supply circuits (figure 1(5) of Kawai) are directly connected to the driving circuit (figure 1(50) of Kawai), said driving circuit shown in detail in figure 2 of Kawai (column 3, lines 21-25 of Kawai). As can clearly be seen in figure 2 of Kawai, the Latch, Data, Clock and STRB signals are directly connected to the appropriate latch or register. The latch and register are connected in parallel to each AND gate that is used to determine which of the heating elements (figure 2($R_1 \ldots R_n$) of Kawai) powered by their associated power transistor (figure 2 ($Q_1 \ldots Q_2$) of Kawai) (column 3, lines 49-62 of Kawai). The arrangement shown in figure 2 of Kawai is a direct arrangement for accessing multiple switchable printing elements. Since the

path is direct, said path therefore shortens a wiring line to each printing element.

Regarding claim 4: Kawai discloses that the data supply circuits (figure 1(5) and column 3, lines 23-25 of Kawai) include a plurality of shift registers (figure 2(17) of Kawai) for receiving clock and data signals (figure 2("DATA","CLOCK") and column 3, lines 53-55 of Kawai), a plurality of latches (figure 2(16) of Kawai) for latching output signals from shift registers (column 3, lines 50-53 of Kawai), and AND circuits (figure 2($A_1 \ldots A_n$) of Kawai) for performing a logical product of outputs from the latches and a driving signal (column 3, lines 55-62 of Kawai). The latch circuit (figure 1(16) of Kawai) comprises multiple latches (column 4, lines 48-51 of Kawai "latched in the latches 16, at the same time supplied to the AND gates"). Further, Kawai teaches in another embodiment using multiple shift registers (figure 20(117a-117c) of Kawai) for multiple data and clock signals to supply the necessary signals to the selected heating elements (figure 20(115) of Kawai) which are energized based on multiple strobe signals (figure 20(119a-119c) and column 18, line 63 to column 19, line 4 of Kawai). The use of multiple shift registers would be obvious to one of ordinary skill in the art at the time of the invention, especially given the combination of Kawai in view of Tamura in which a printing element is driven in each of a plurality of groups of printing elements (column 5, lines 49-51 and column 6, lines 16-20 of Tamura). If there are multiple groups or divisions of printing, such as in Tamura or as shown in figure 20 of Kawai, then one of ordinary skill in the art would use multiple shift registers.

Regarding claim 5: Kawai discloses that the printhead includes an inkjet printhead (figure 27(202) of Kawai) for printing data by discharging ink (column 24, lines 50-52 and lines 58-61 of Kawai).

Regarding claim 6: Kawai discloses that the printhead includes a printhead for discharging the ink using thermal energy (column 4, lines 56-62 of Kawai) and an electrothermal transducer (figure 2(15) of Kawai) for generating thermal energy to be applied to the ink (column 4, lines 50-55 of Kawai).

Regarding claim 7: Kawai discloses a head cartridge (figure 1 of Kawai) comprising a printhead (figure 1 of Kawai) in which a plurality of printing elements (figure 1 (10) and column 3, lines 34-36 of Kawai) arranged in a predetermined direction (column 3, lines 29-33 of Kawai) and a driving circuit (figure 1(50) of Kawai) for driving the printing elements (column 4, lines 35-41 of Kawai) are formed on a single substrate (figure 1 and figure 2 of Kawai). The thermal head (figure 1(10) of Kawai) contains a plurality of printing elements since said thermal head prints a plurality of primary colors (column 3, lines 29-36 of Kawai). Said printing elements are set according to specific positions (column 3, lines 29-33 of Kawai), and therefore must be set in a predetermined direction. The plurality of printing elements (figure 1 (10) of Kawai) are shown in figure 2 of Kawai (column 2, lines 15-16 of Kawai), and are clearly one a single substrate.

Kawai further discloses that said printhead includes data supply circuits (figure 1(5) of Kawai) for supplying driving data to the driving circuit (column 4, lines 45-48 of Kawai) for driving each printing element through any of a plurality of paths (column 4, lines 47-55 of Kawai). Said data supply

circuits are a part of the overall directly connected digital logic circuitry (figure 1 and column 3, lines 21-25 of Kawai). Therefore, said data supply circuits are arranged on the substrate.

Kawai further discloses an ink tank for storing ink to be supplied to the printhead (column 24, lines 58-60 of Kawai).

Kawai does not disclose expressly that the printing elements are classified into a plurality of groups; and a selection circuit which is common to the plurality of groups and selects a printing element to be driven in each group, wherein said selection circuit is arranged on the substrate.

Tamura discloses classifying printing elements into a plurality of groups (column 5, lines 44-51 of Tamura); and a selection circuit (figure 2 of Tamura) which is common to the plurality of groups (column 5, lines 19-20 of Tamura) and selects a printing element to be driven in each group (column 5, lines 49-51 and column 6, lines 16-20 of Tamura).

Kawai and Tamura are combinable because they are from the same field of endeavor, namely the digital control of printheads and printhead data. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the plurality of groups and a selection circuit to select a printing element from each group, as taught by Tamura, in the overall printhead taught by Kawai. Since the printhead of Kawai is a single integrated device (figure 1 of Kawai), the selection circuit taught by Tamura would also be arranged on the substrate, said substrate being the substrate that is inherently required to form a physical digital circuit. The motivation for doing so would have been that constant switching of power components creates a large power loss and requires bulky

circuits (column 2, lines 44-57 of Tamura) and using a diode or transistor matrix requires a disadvantageous number of wiring lines, which increases cost and degrades reliability (column 2, line 58 to column 3, line 7 of Tamura). Both of these problems are solved by using the selection circuit taught by Tamura (column 3, lines 11-14 of Tamura). Therefore, it would have been obvious to combine Tamura with Kawai to obtain the invention as specified in claim 7.

Regarding claim 8: Kawai discloses a printing apparatus (figure 1 of Kawai) for printing data by using a printhead (figure 1 of Kawai) in which a plurality of printing elements (figure 1 (10) and column 3, lines 34-36 of Kawai) arranged in a predetermined direction (column 3, lines 29-33 of Kawai) and a driving circuit (figure 1(50) of Kawai) for driving the printing elements (column 4, lines 35-41 of Kawai) are formed on a single substrate (figure 1 and figure 2 of Kawai). The thermal head (figure 1(10) of Kawai) contains a plurality of printing elements since said thermal head prints a plurality of primary colors (column 3, lines 29-36 of Kawai). Said printing elements are set according to specific positions (column 3, lines 29-33 of Kawai), and therefore must be set in a predetermined direction. The plurality of printing elements (figure 1 (10) of Kawai) are shown in figure 2 of Kawai (column 2, lines 15-16 of Kawai), and are clearly one a single substrate.

Kawai further discloses that said printhead includes data supply circuits (figure 1(5) of Kawai) for supplying driving data to the driving circuit (column 4, lines 45-48 of Kawai) for driving each printing element through any of a plurality of paths (column 4, lines 47-55 of Kawai). Said data supply circuits are a part of the overall directly connected digital

logic circuitry (figure 1 and column 3, lines 21-25 of Kawai). Therefore, said data supply circuits are arranged on the substrate.

Kawai further driving data generation means (figure 1(6) and column 3, lines 36-38 of Kawai) for generating a data signal for each path of the data supply circuit (column 3, lines 38-45 of Kawai). The driving data generation means (figure 1(6) of Kawai) controls the overall apparatus (column 3, lines 36-38 of Kawai), and thus the reading of the temperature data from the ROM and the tonal data from the density counter, which is used to control the driving of the printhead (column 3, lines 38-45 of Kawai).

Kawai does not disclose expressly that the printing elements are classified into a plurality of groups; and a selection circuit which is common to the plurality of groups and selects a printing element to be driven in each group, wherein said selection circuit is arranged on the substrate.

Tamura discloses classifying printing elements into a plurality of groups (column 5, lines 44-51 of Tamura); and a selection circuit (figure 2 of Tamura) which is common to the plurality of groups (column 5, lines 19-20 of Tamura) and selects a printing element to be driven in each group (column 5, lines 49-51 and column 6, lines 16-20 of Tamura).

Kawai and Tamura are combinable because they are from the same field of endeavor, namely the digital control of printheads and printhead data. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the plurality of groups and a selection circuit to select a printing element from each group, as taught by Tamura, in the overall printhead taught by Kawai. Since the printhead of Kawai

is a single integrated device (figure 1 of Kawai), the selection circuit taught by Tamura would also be arranged on the substrate, said substrate being the substrate that is inherently required to form a physical digital circuit. The motivation for doing so would have been that constant switching of power components creates a large power loss and requires bulky circuits (column 2, lines 44-57 of Tamura) and using a diode or transistor matrix requires a disadvantageous number of wiring lines, which increases cost and degrades reliability (column 2, line 58 to column 3, line 7 of Tamura). Both of these problems are solved by using the selection circuit taught by Tamura (column 3, lines 11-14 of Tamura). Therefore, it would have been obvious to combine Tamura with Kawai to obtain the invention as specified in claim 8.

Regarding claim 9: Kawai discloses a printhead element substrate (figure 1 of Kawai) in which a plurality of printing elements (figure 1 (10) and column 3, lines 34-36 of Kawai) arranged in a predetermined direction (column 3, lines 29-33 of Kawai) and a driving circuit (figure 1(50) of Kawai) for driving the printing elements (column 4, lines 35-41 of Kawai) are formed on a single substrate (figure 1 and figure 2 of Kawai). The thermal head (figure 1(10) of Kawai) contains a plurality of printing elements since said thermal head prints a plurality of primary colors (column 3, lines 29-36 of Kawai). Said printing elements are set according to specific positions (column 3, lines 29-33 of Kawai), and therefore must be set in a predetermined direction. The plurality of printing elements (figure 1 (10) of Kawai) are shown in figure 2 of Kawai (column 2, lines 15-16 of Kawai), and are clearly one a single substrate.

Kawai further discloses that said printhead includes data supply circuits (figure 1(5) of Kawai) for supplying driving data to the driving circuit (column 4, lines 45-48 of Kawai) for driving each printing element through any of a plurality of paths (column 4, lines 47-55 of Kawai). Said data supply circuits are a part of the overall directly connected digital logic circuitry (figure 1 and column 3, lines 21-25 of Kawai). Therefore, said data supply circuits are arranged on the substrate.

Kawai does not disclose expressly that the printing elements are classified into a plurality of groups; and a selection circuit which is common to the plurality of groups and selects a printing element to be driven in each group, wherein said selection circuit is arranged on the substrate.

Tamura discloses classifying printing elements into a plurality of groups (column 5, lines 44-51 of Tamura); and a selection circuit (figure 2 of Tamura) which is common to the plurality of groups (column 5, lines 19-20 of Tamura) and selects a printing element to be driven in each group (column 5, lines 49-51 and column 6, lines 16-20 of Tamura).

Kawai and Tamura are combinable because they are from the same field of endeavor, namely the digital control of printheads and printhead data. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the plurality of groups and a selection circuit to select a printing element from each group, as taught by Tamura, in the overall printhead taught by Kawai. Since the printhead of Kawai is a single integrated device (figure 1 of Kawai), the selection circuit taught by Tamura would also be arranged on the substrate, said substrate being the substrate that is inherently

required to form a physical digital circuit. The motivation for doing so would have been that constant switching of power components creates a large power loss and requires bulky circuits (column 2, lines 44-57 of Tamura) and using a diode or transistor matrix requires a disadvantageous number of wiring lines, which increases cost and degrades reliability (column 2, line 58 to column 3, line 7 of Tamura). Both of these problems are solved by using the selection circuit taught by Tamura (column 3, lines 11-14 of Tamura). Therefore, it would have been obvious to combine Tamura with Kawai to obtain the invention as specified in claim 9.

14. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai (US Patent 5,539,433) in view of Tamura (European Patent Application Publication EP 0 811 488 A2) and obvious design choice.

Regarding claim 3: Kawai discloses the data supply circuits (figure 1(5) of Kawai) which are arranged in the circuit diagram of figure 1 of Kawai. Kawai in view of Tamura does not disclose expressly that said data supply circuits are arranged on two sides of a printing element array. However, figure 1 of Kawai is a block diagram of the printer circuitry (column 2, lines 13-14 of Kawai) and is thus only representative of the electrical circuitry. Figure 1 of Kawai does not specifically have to represent the exact physical arrangement of the circuitry. Since the printhead taught by Kawai in view of Tamura comprises a plurality of groups, with a printing element of each group selected to be driven (column 5, lines 49-51 and column 6, lines 16-20 of Tamura), it would have been an obvious engineering design choice to one of ordinary skill in the art at

the time of the invention to arrange the data supply circuits on two sides of a printing element array. Minimizing the amount of wiring required is a desired characteristic specifically taught in Tamura (column 2, line 58 to column 3, line 7 of Tamura) and is also generally considered good circuit design practice by those of ordinary skill in the art. By placing the data supply circuits on two sides of a printing element array, each printing element array is directly connected with a minimum of required wiring, thus accomplishing the desired circuit characteristics taught by Tamura and maintaining generally accepted circuit design practice.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Takamura et al., US Patent 6,493,109 B1, 10 December 2002.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James A Thompson whose telephone number is 703-305-6329. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David K Moore can be reached on 703-308-7452. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James A. Thompson
Examiner
Art Unit 2624

JAT
15 February 2005

THOMAS LEE
PRIMARY EXAMINER